PCIe® Differential Vias Design to Reduce Inter-Differential Pair Crosstalk

Vinod Arjun Huddar

Sr. Signal Integrity Engineer

Seagate Technology HDD

Disclaimer

Presentation Disclaimer: All opinions, judgments, recommendations, etc. that are presented herein are the opinions of the presenter of the material and do not necessarily reflect the opinions of the PCI-SIG®.

Key Contributors

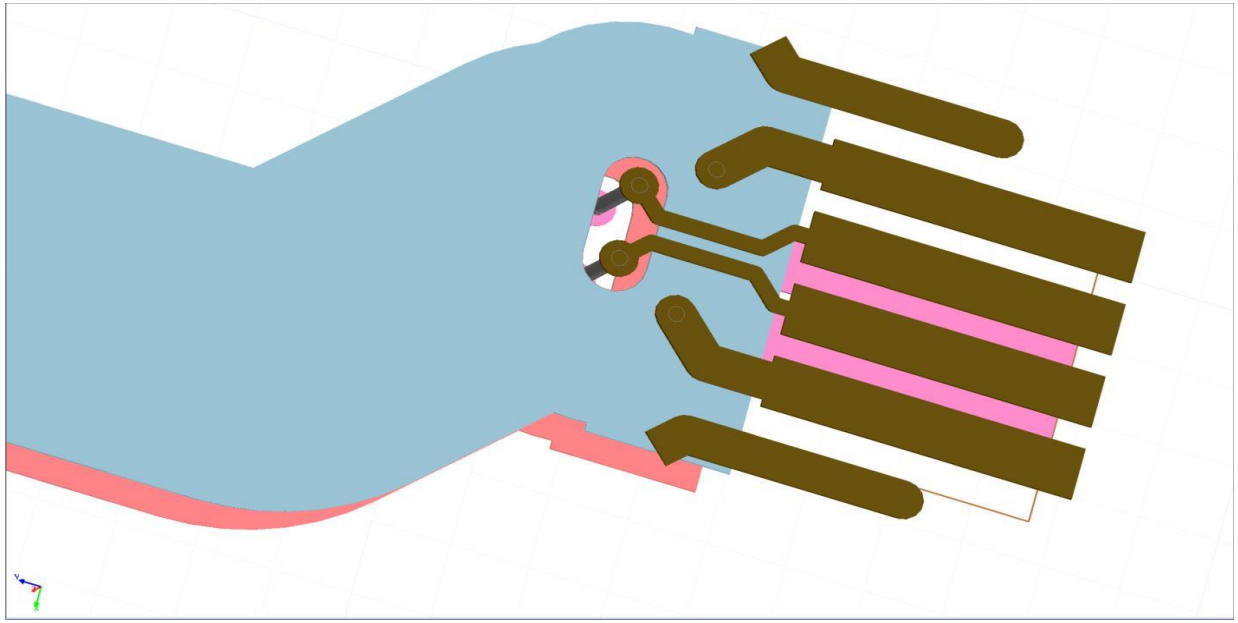
- **Satish Pratapneni: Director of Hardware Engineering, Seagate Technology HDD India Pvt Ltd**

Topics

- **Typical PCIe® Via Designs**
  - Widely Used PCIe Vias Design
  - Differential Vias in Parallel & Crosstalk
- **Proposed PCIe Via Design**
  - Proposed Vias Design
  - Crosstalk Reduction in Inter-pair Vias
- **Summary**

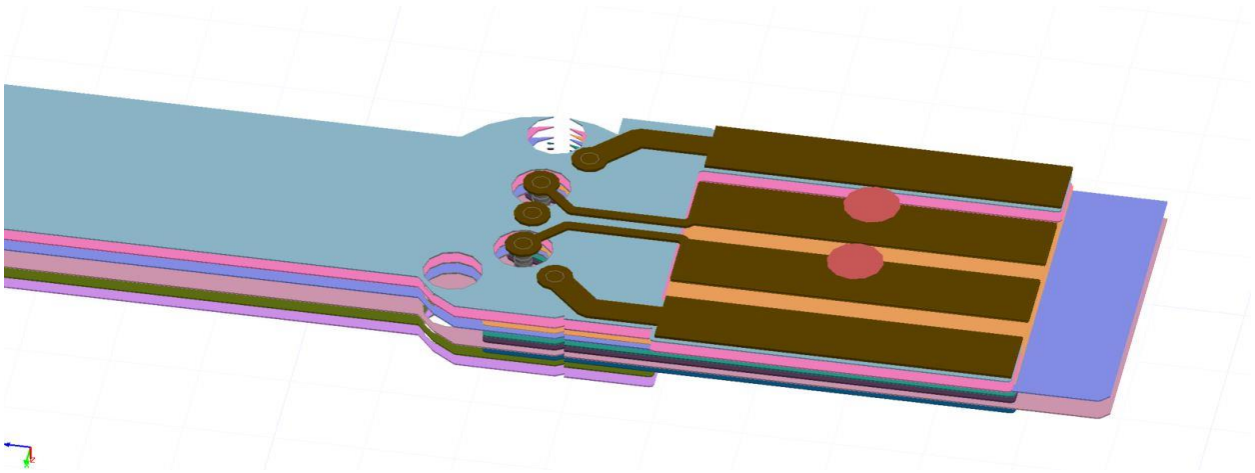
Typical PCIe Vias

- **Typical PCIe Via Designs**
  - PCIe Differential Vias are typically routed as shown below.
  - In these designs the traces spread apart before entering via.
  - This causes differential impedance to increase at via.



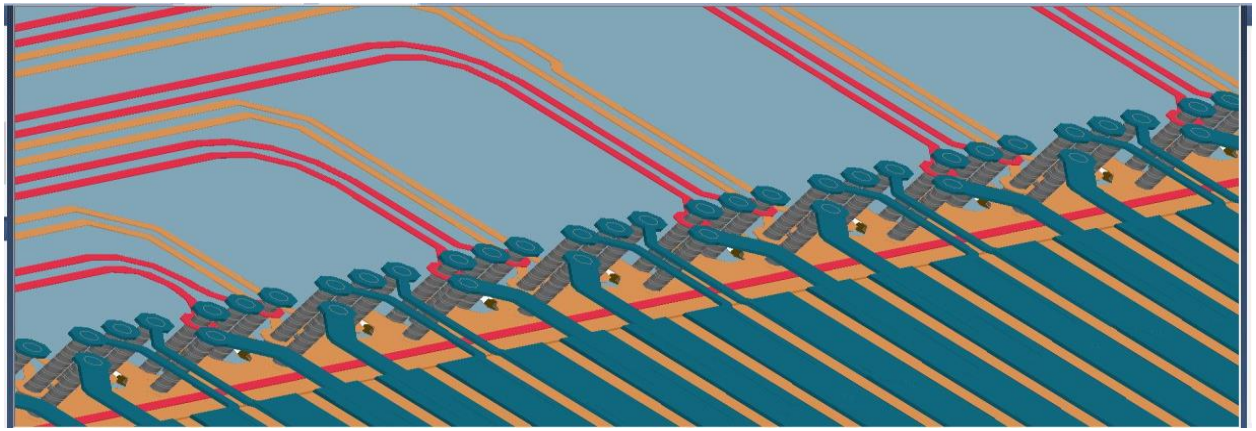
Typical PCIe Vias

- **Few more PCIe Via Designs**
  - Another via approach followed is to add a ground via in between differential vias. Adding ground vias provide a vertical return reference for each of the 2 signal vias.
  - In this approach single ended via impedance is lesser than typical 50 Ohms so that differential via impedance also becomes lesser i.e. 85 ohms instead of 100 ohms.



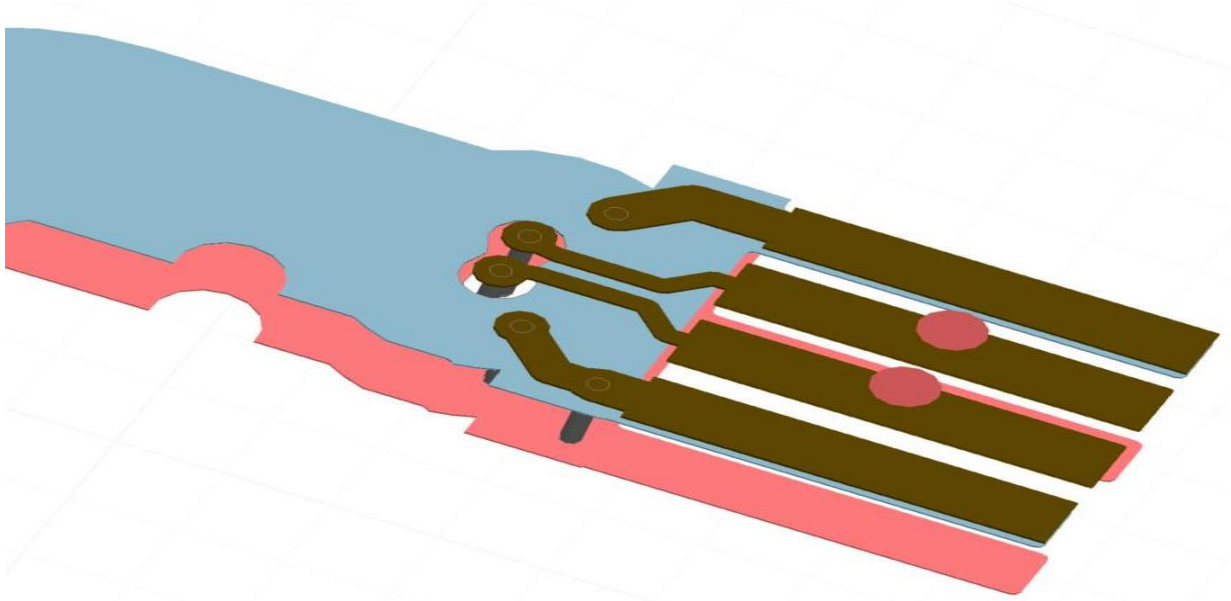
Differential Vias in Parallel & Crosstalk

- **Differential Vias in Parallel & Crosstalk**
  - It is usual to have multiple differential vias in parallel like PCIe x16 interface. Differential via-2-via crosstalk is an concern as differential vias come in parallel to each other vertically.
  - Crosstalk control is done typically by adding more ground vias around differential vias or placing the differential vias farther apart.



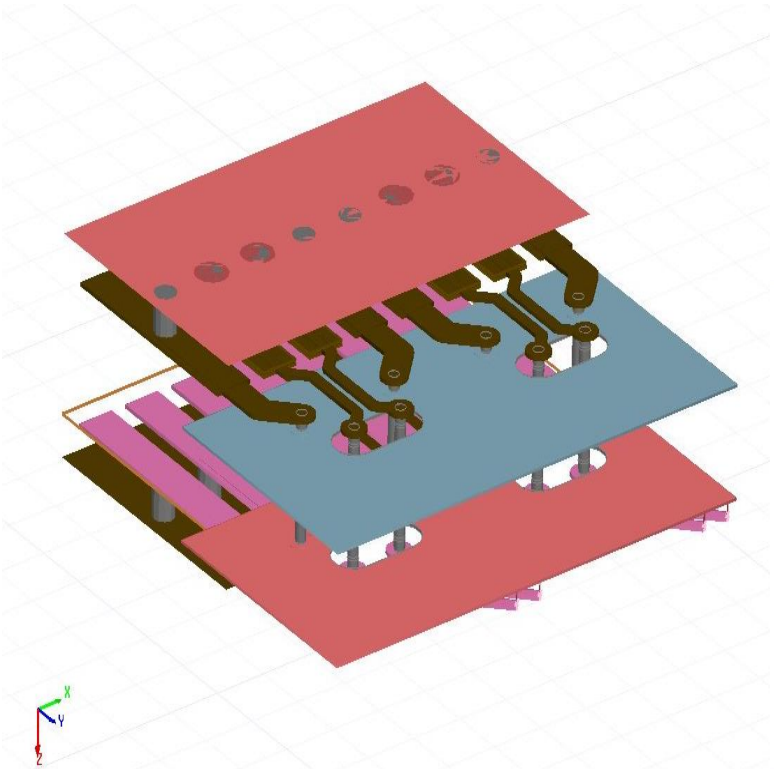
Proposed Differential Via Structure

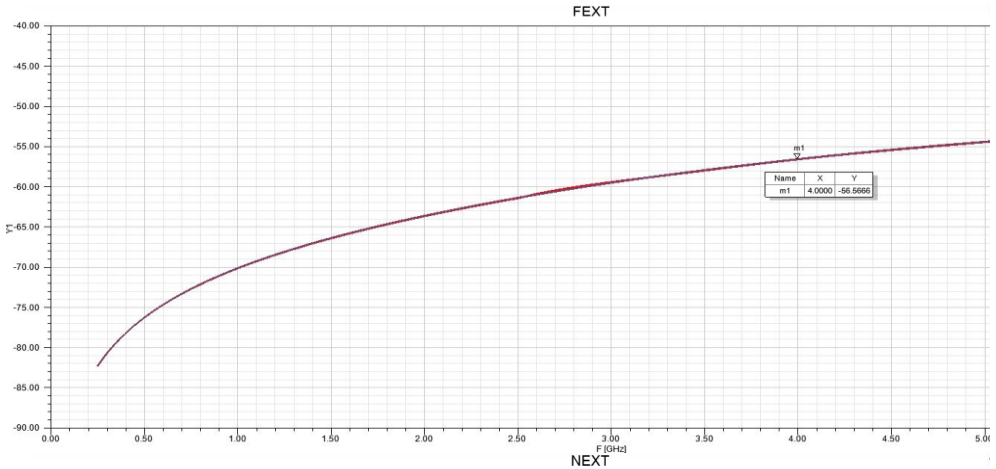
- **Proposed PCIe Via Designs**
  - PCIe Differential Vias are tightly coupled as shown below.
  - In these designs the traces do not spread apart before entering via.
  - This causes differential impedance not to increase at via.

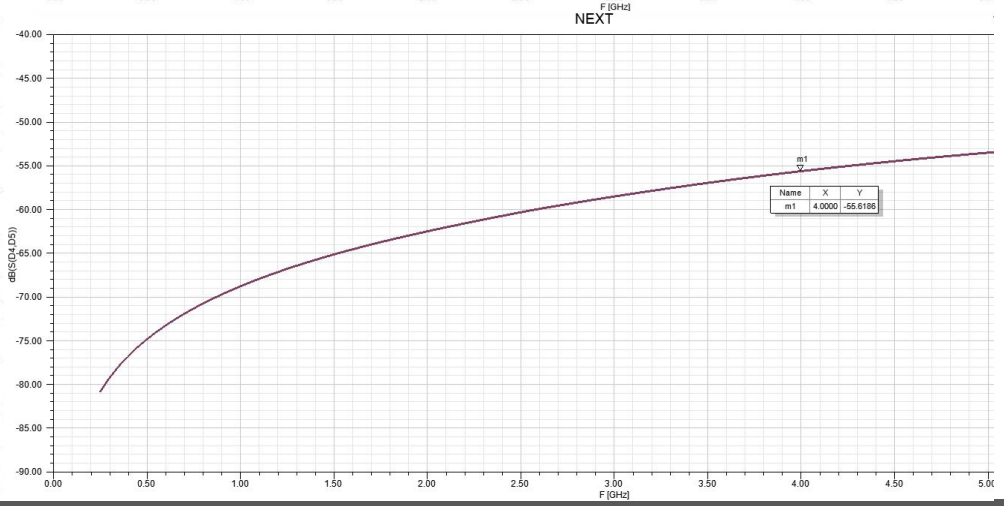


Typical Differential Vias Crosstalk

- **Typical Vias in Parallel & Crosstalk**
  - FEXT @4GHz is at -56dB
  - NEXT @4GHz is at -55dB

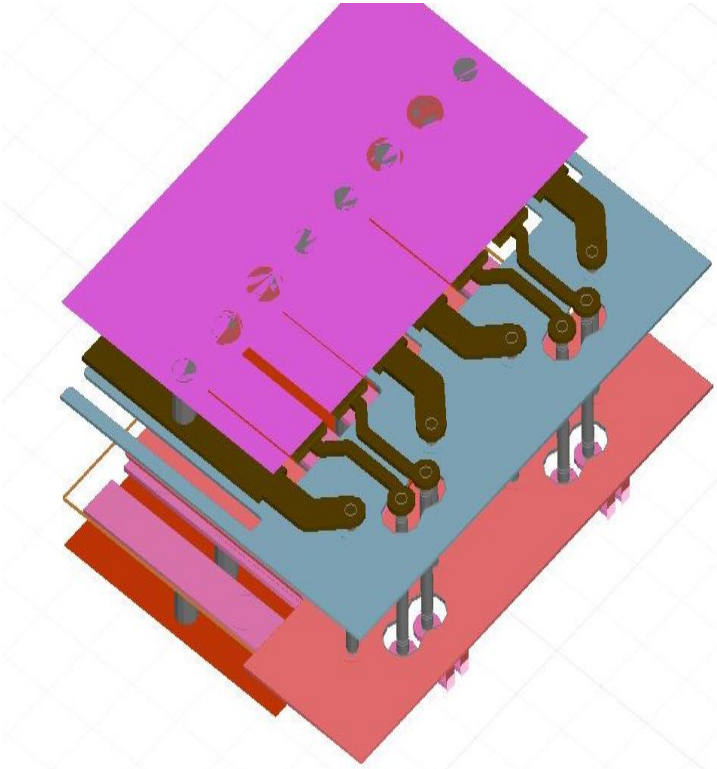


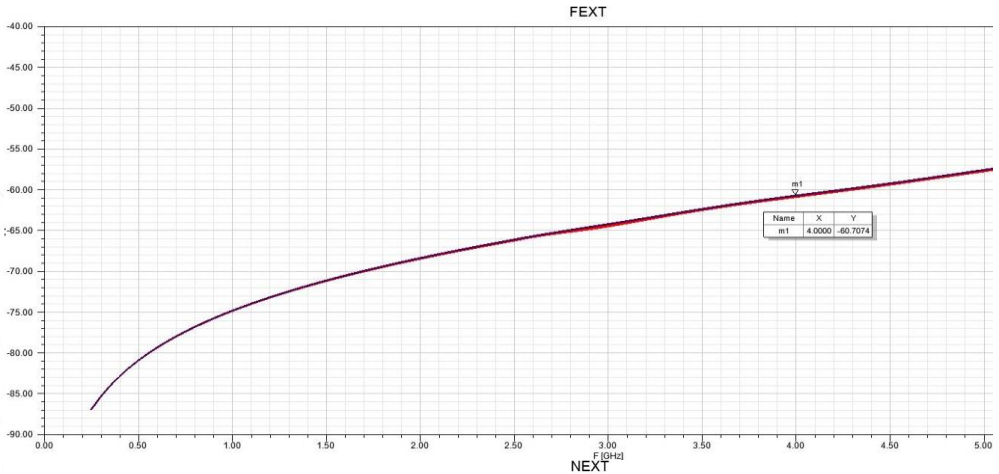


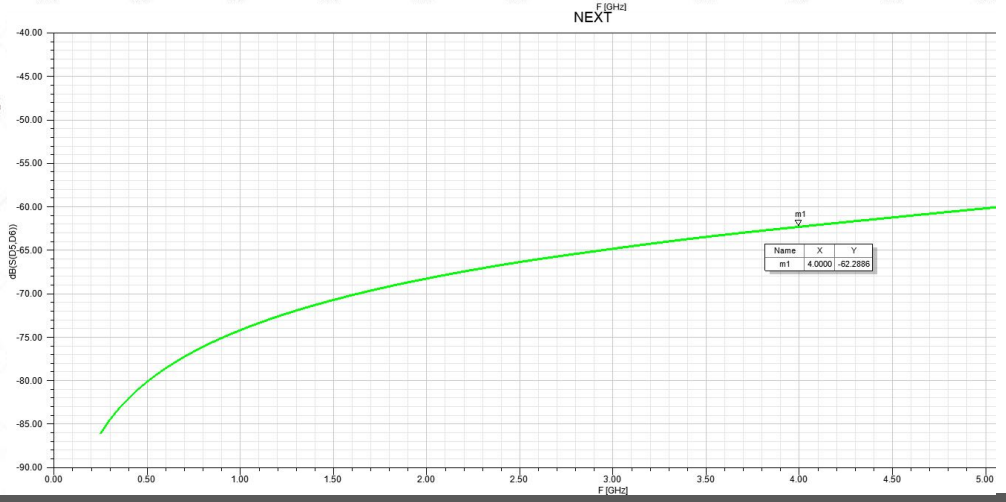


Proposed Differential Vias Crosstalk

- **Proposed Vias in Parallel & Crosstalk**
  - FEXT @4GHz is at -60dB
  - NEXT @4GHz is at -62dB

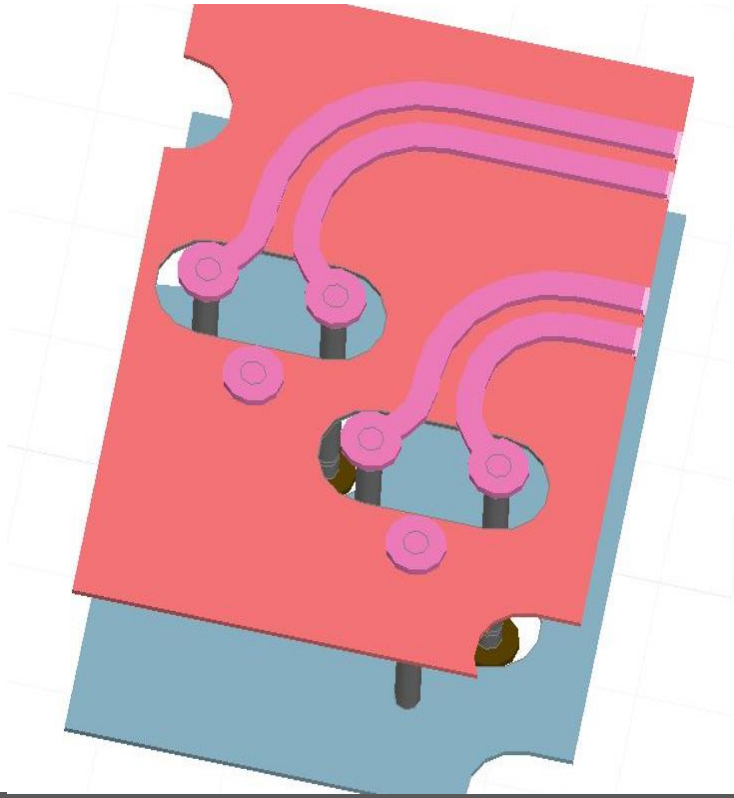


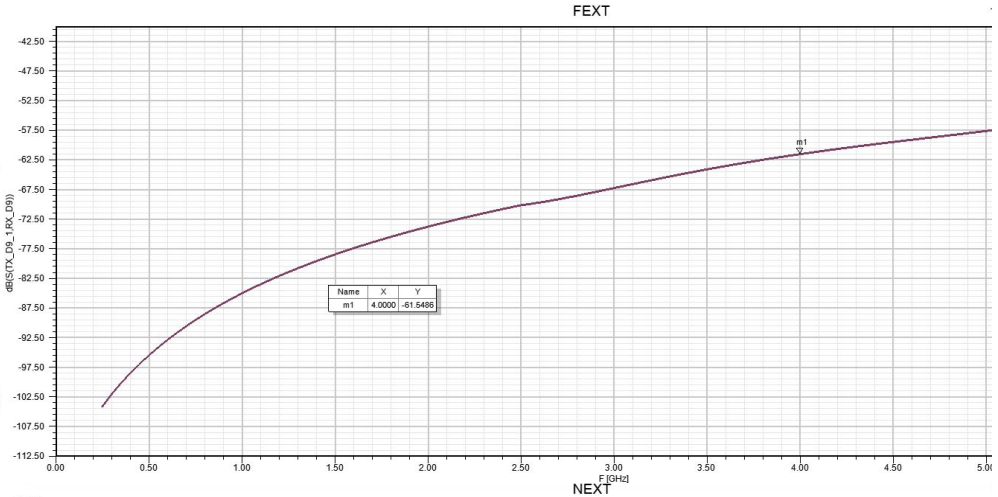


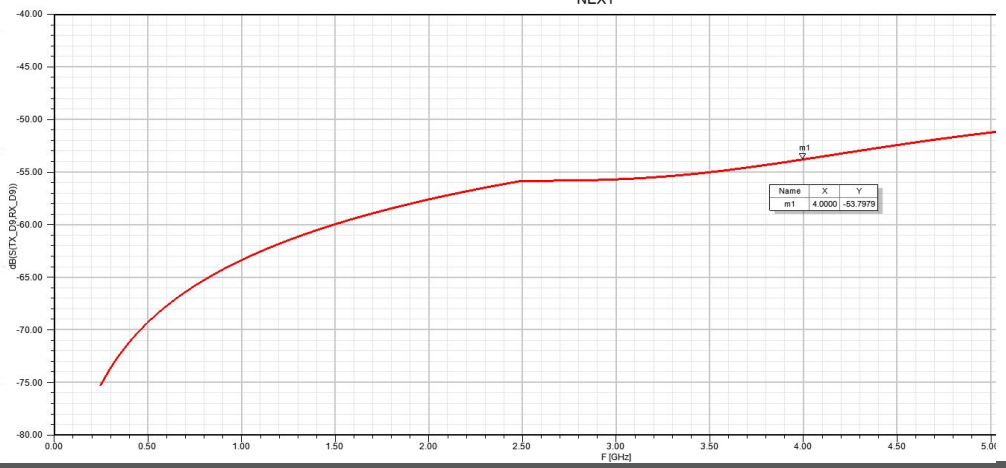


Typical Differential Vias Crosstalk

- **Typical Vias in Parallel & Crosstalk**
  - FEXT @4GHz is at -61dB
  - NEXT @4GHz is at -53dB

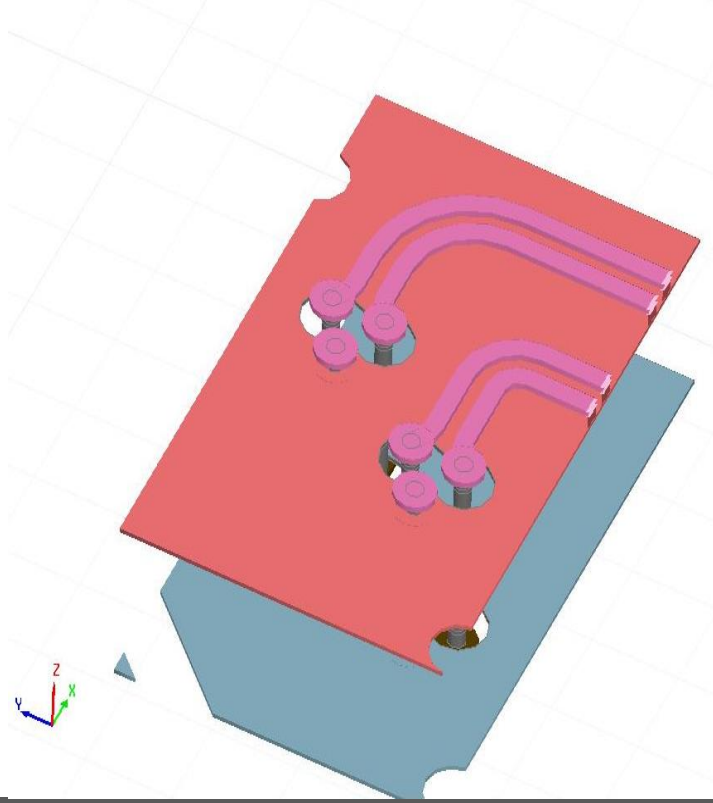


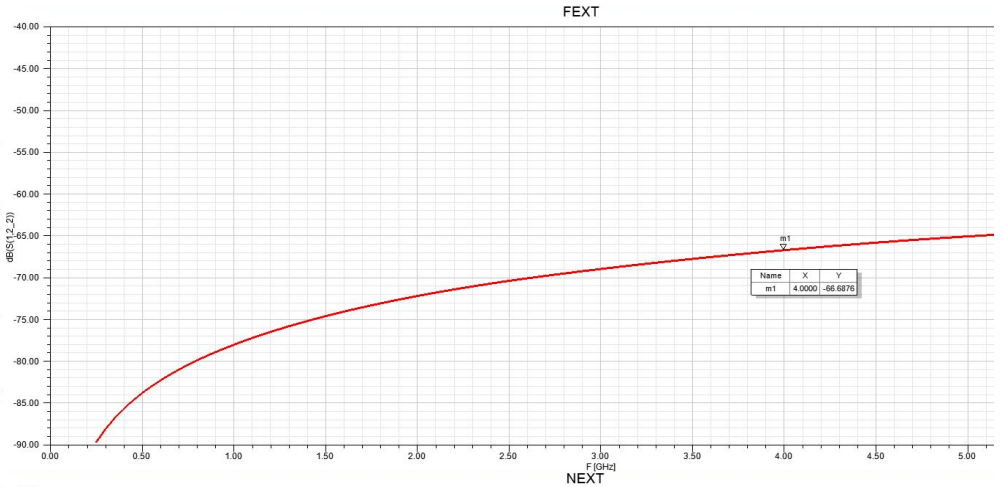


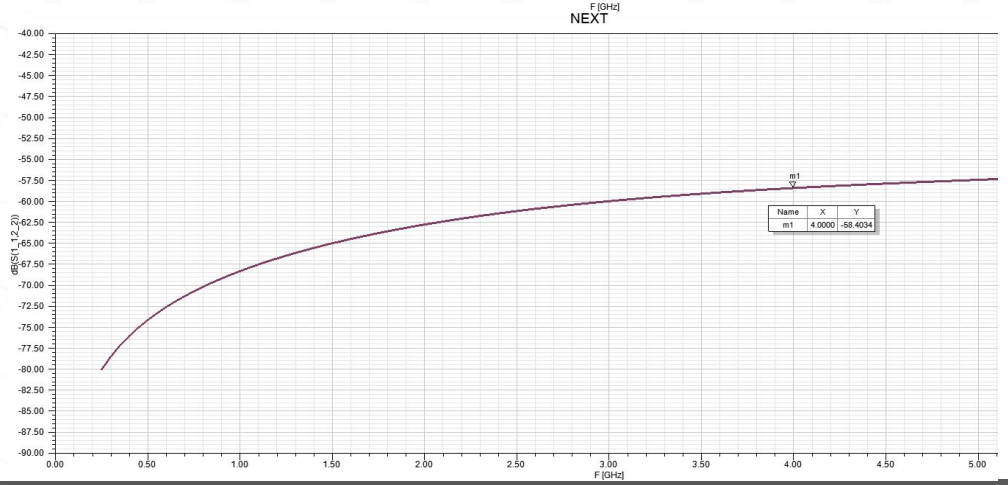


Proposed Differential Vias Crosstalk

- **Proposed Vias in Parallel & Crosstalk**
  - FEXT @4GHz is at -66dB
  - NEXT @4GHz is at -58dB

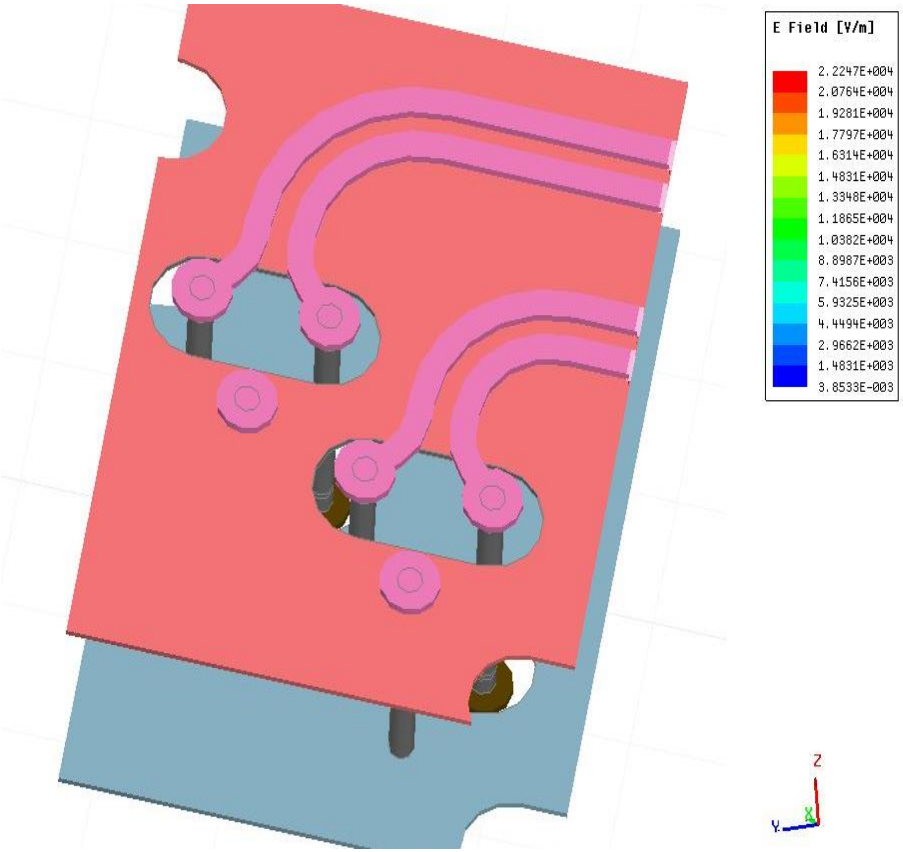


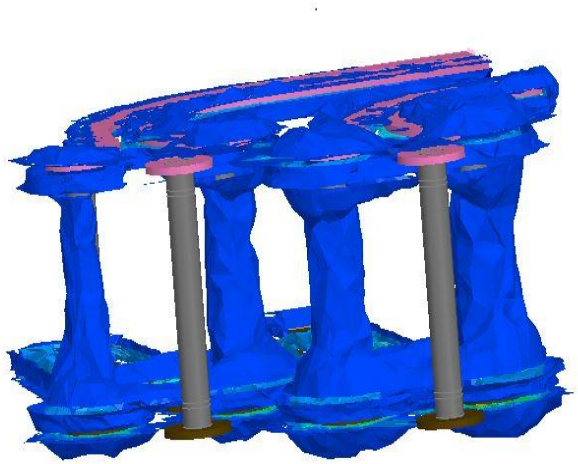




Typical Differential Vias E Field

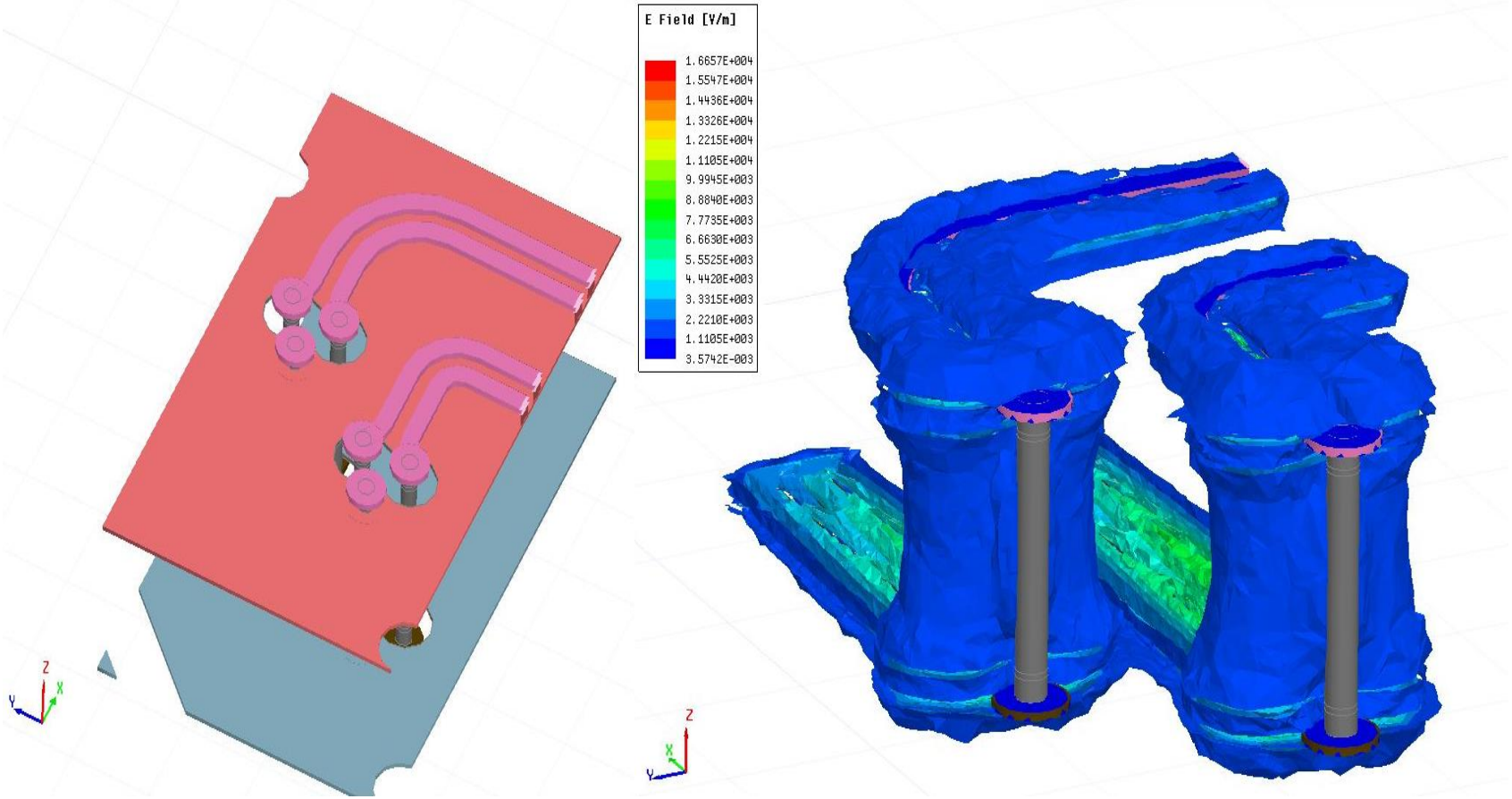
- **Typical Vias in Parallel & E Field**





Proposed Differential Vias E Field

- **Proposed Vias in Parallel & E Field**



Summary

- **Advantages**
  - Vias are tightly EM coupled thus retaining all the advantages of differential routing.
  - Tightly coupled Vias causes less EM fields to near-by Vias resulting in reduced interference/crosstalk.

- **FEXT NEXT Comparison**
  - Near Gold Fingers, there is improvement of > 4dB with new via structure.
  - Transition vias in PCB show > 5dB improvement with new via structure.

References

- Chunfei Ye, Xiaoning Ye and Enrique Lopez Miralrio “Via Pattern Design and Optimization for Differential Signaling 25Gbps and Above”, 2016 IEEE International Symposium on Electromagnetic Compatibility (EMC).
- K.Aihara, et al, “Minimizing differential crosstalk of vias for high speed data transmission”, IEEE EPEPS, 2014, Portland, Oregon, USA.
- Wei Yao, et al, “Design of Package BGA Pin-out for >25Gb/s High Speed Serdes Considering PCB Via Crosstalk”, 2015 IEEE Symposium on EMC-SI, Santa Clara, USA.
- Yujeong Shim and Dan Oh, “Improved PCB Via Pattern to reduce crosstalk at Package BGA Region for High Speed Serial Interface”, 2014, IEEE ECTC, Orlando, USA.
- M. Wang, X. Ye, et al, “System Level Impact of stiching Vias and Capacitors for High Speed Differential Links”, Electronic Components and Technology Conference, 2007.
- Yalin Guan, Shilel Zhou, “ The Use of Taguchi Method for Robust Optimization of PCB Differential-Via “, 2013, IEEE Microwave Technology & Computational Electromagnetics International Conference, Qingdao, China.
- Alma Jaze, Bruce Archambeault, Sam Connor, “Differential Mode to Common Mode Conversion on Differential Signal Vias due to Asymmetric GND Via Configurations”, IEEE EMC Symposium 2013.

Thank you for attending the PCI-SIG Developers Conference Israel 2017.

For more information please go to www.pcisig.com